CC3551E
WiFi and Bluetooth Module Hardware Specification

Version：V1.1

2025/10/15

CONTENTS

1. Module Overview

1.1. Description

The CC3551E module is a WIFI+ Bluetooth dual-in-one wireless module designed based on CC3551E as the core. Wifi supports MAC, baseband and RF transceivers of IEEE 802.11b /g/n/ax at 2.4GHz and 5GHz, single-stream 20MHz channel, application throughput up to 20Mbps (UDP), hardware-based encryption and decryption, and supports WPA2 and WPA3. Supports 4-bit SDIO or SPI host interfaces. Bluetooth supports low-power Bluetooth® 5.4, LE encoding PHY (long range), LE 2M PHY (high speed), and broadcast extensions. The module is packaged with 18-pin stamp holes.

1.2. Applications

• Building automation thermostats - HVAC motor control - Wireless security cameras - video doorbells - garage door systems

• Appliances: Refrigerator and freezer - oven - washing machine and dryer - Household water heater - indoor air conditioner - coffee machine - Sweeping robot - lawn mower robot

• Power grid infrastructure electricity meters - series inverters - micro-inverters - battery energy storage systems - electric vehicle charging infrastructure

• Medical infusion pumps - Electronic hospital beds and bed controllers - multi-parameter patient monitors - CPAP ventilators - telemedicine systems - Ultrasound scanners - ultrasound intelligent detectors

1.3. Key Features

- Wi-Fi 6 (802.11ax);
- 2.4GHz and 5GHz Wi-Fi 6 and low-power Bluetooth 5.4 matching IC;
- Complete software development kit with open source TCP/IP and TLS stacks;
- Integrated with 2.4GHz PA, it is suitable for a complete wireless solution with an output power up to +20dBm;
- Operating temperature：-40°C to +85°C;
- Application throughput 20Mbps;

  Enhanced security
  - Initial security programming
  - Clean boot
  - Software IP and clone protection
  - Debugging security is achieved through JTAG and debugging port locking
  - An OTP capable of programming the root of trust public key
  - Secure over-the-air (OTA) updates
  - Anti-rollback protection
- Multi-role support (for example, concurrent STA and AP), which can connect Wi-Fi devices on different radio frequency channels (Wi-Fi networks)
- Power management

  –VIO：1.8V OR 3.3V（The default is 3.3V only.）

  –VBAT：3.0V TO 3.6V

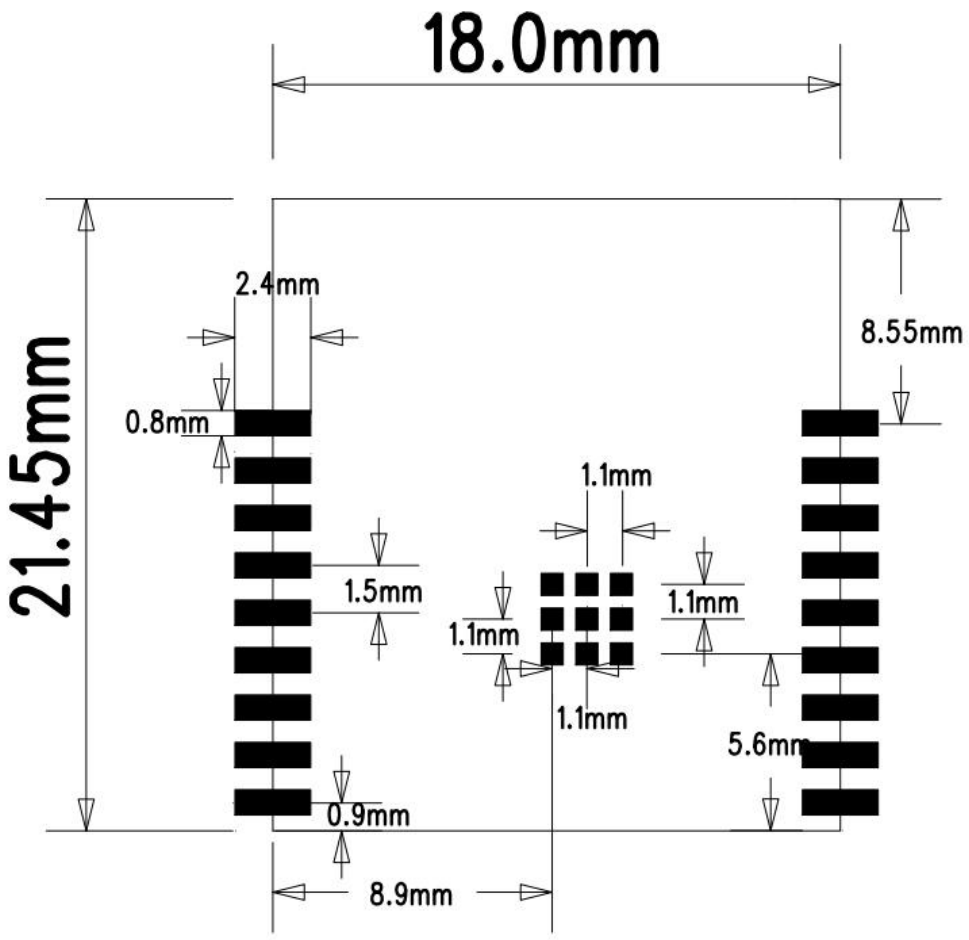
2. Hardware Description

Part number (P/N)	Hardware model	Instructions
	SR-355101PC2N	PCB antenna with a shielding cover
	SR-355102IC2N	IPEX with a shielding cove

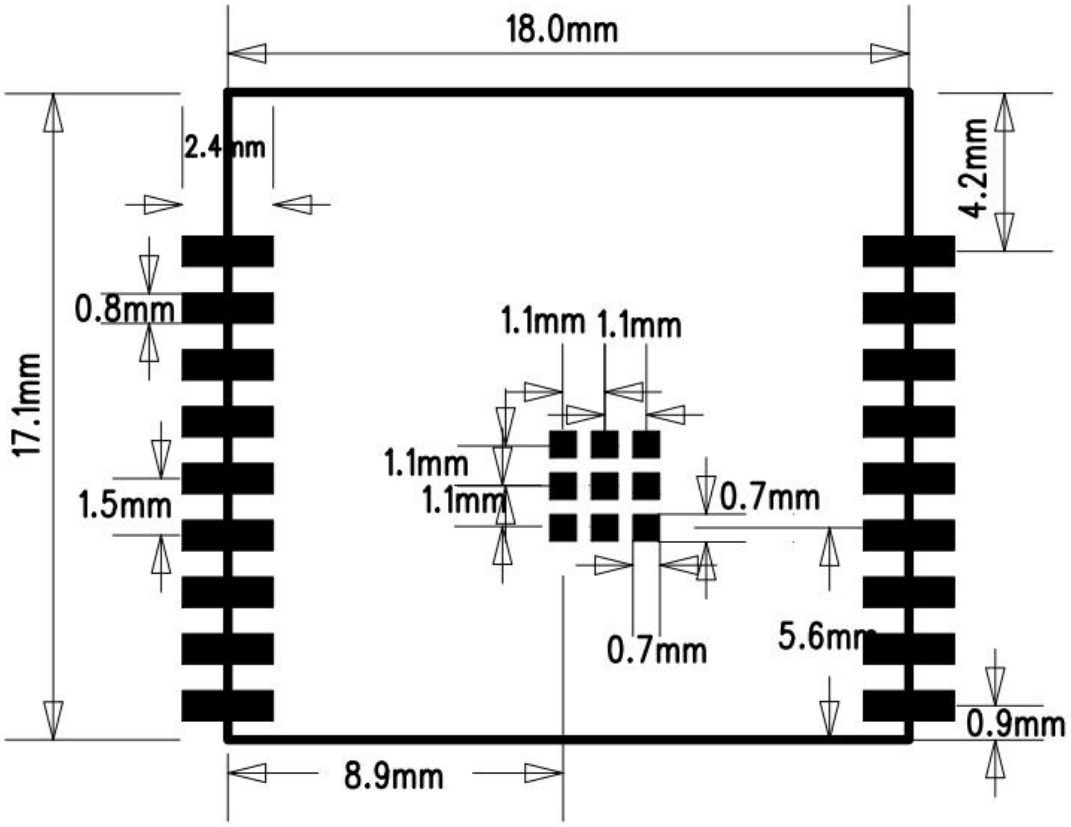
2.1. PCB Dimension Size

2.1.1. SR-355101PC2N (21.45*18*2.7 mm ±0.2mm)/
SR-355102IC2N (17.1*18*2.7 mm ±0.2mm) Size

SR-355101PC2N（top view）



SR-355102IC2N（top view）



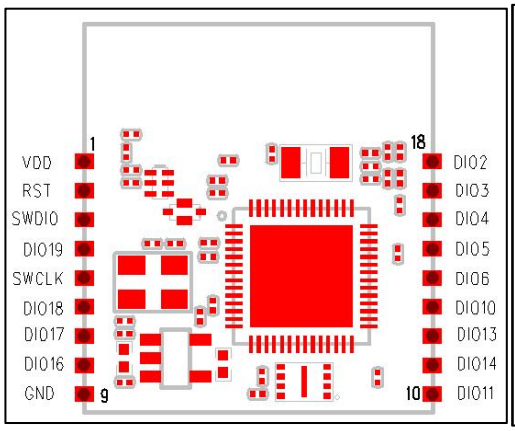
2.1.2、SR-355101PC2N/SR-355102IC2N Module picture.

SR-355101PC2N

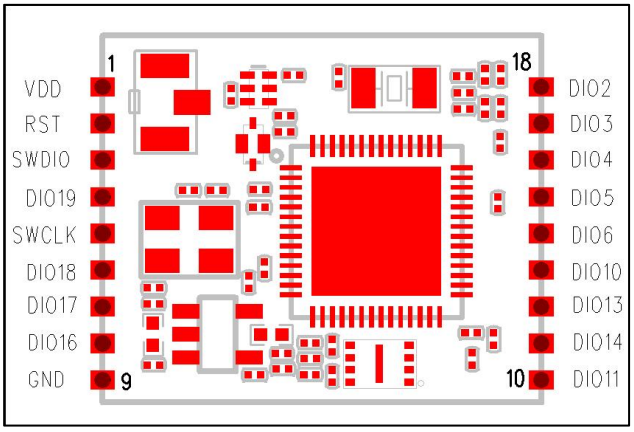
SR-355102IC2N

2.1.3、SR-355101PC2N/SR-355102IC2N Pins

SR-355101PC2N



SR-355102IC2N



2.1.4 、Pin Definition

PIN	Name	PAD type	Description
1	VDD	P	power supply input
2	RST	I	Reset line for enabling or disabling device (active low)
3	SWDIO	I/O	GPIO, SWD interface: mode select or SWDIO,
4	DIO19	I/O	GPIO,SPI0_PICO
5	SWCLK	O	GPIO,SWD interface: clock
6	DIO18	I/O	GPIO,SPI0_POCI
7	DIO17	I/O	GPIO,SPI0_CLK
8	DIO16	I/O	GPIO,SPI0_CS1
9	GND	-	Ground
10	DIO11	I/O	GPIO,SDIO_D2
11	DIO14	I/O	GPIO,UART0_RX
12	DIO13	I/O	GPIO,UART0_TX
13	DIO10	I/O	GPIO,SDIO_D3
14	DIO6	I/O	GPIO,SDIO_D1
15	DIO5	I/O	GPIO,SDIO_D0
16	DIO4	I/O	GPIO,SDIO_CMD
17	DIO3	I/O	GPIO,SDIO_CLK
18	DIO2	I/O	GPIO,SDIO_OOB_IRQ

GPIO No.	SIGNAL NAME	SIGNAL TYPE [1]	IO RING	PIN MUX ENCODING	PAD STATES	
					RESET	LPDS [2]
GPIO2	ADC6	I/O	VIO1		PU	Hi-Z, Pull, Drive
	xSPI_RESET_RAM			1		
	SDMMC_CD			3		
	I2C1_CLK			6		
	GPT1_3			9		
	DCAN_TX			10		
	SPI0_CS4			16		
	GPT1_PRE_EVENT			18		
	SDIO_OOB_IRQ			19		
	COEX_GRANT			20		
	COEX_REQ			21		
	CCA			24		

GPIO No.	SIGNAL NAME	SIGNAL TYPE [1]	IO RING	PIN MUX ENCODING	PAD STATES	
					RESET	LPDS [2]
GPIO4	ADC4	I/O	VIO1		PU	Hi-Z, Pull, Drive
	UART1_RX			1		
	SDMMC_CD			3		
	SPI1_CS1			4		
	UART1_CTS			5		
	I2S_BCLK			6		
	I2S_DATA1			7		
	PDM_BCLK			8		
	GPT1_1			9		
	DCAN_TX			10		
	SPI0_CS2			16		
	GPT1_0_N			18		
	SDIO_CMD			19		
	COEX_PRIORITY			20		
	GPT0_1_N			21		
	I2C1_CLK			28		
GPIO3	ADC5	I/O	VIO1		PU	Hi-Z, Pull, Drive
	UART1_TX			1		
	SDMMC_WP			3		
	SPI1_CLK			4		
	UART1_RTS			5		
	I2S_MCLK			6		
	I2S_DATA0			7		
	PDM_DATA1			8		
	GPT1_0			9		
	DCAN_RX			10		
	SPI0_CS3			16		
	xSPI_CS_RAM			17		
	GPT1_1_N			18		
	SDIO_CLK			19		
	COEX_REQ			20		
	GPT0_0_N			21		
	GPT_INFRARED			22		
	I2C1_DATA			28		

GPIO No.	SIGNAL NAME	SIGNAL TYPE [1]	IO RING	PIN MUX ENCODING	PAD STATES	
					RESET	LPDS [2]
GPIO6	ADC2	I/O	VIO1		PU	Hi-Z, Pull, Drive
	xSPI_CS_RAM			1		
	SDMMC_POW1			3		
	SPI1_PICO			4		
	UART1_RX			5		
	I2C0_DATA			6		
	I2S_WCLK			7		
	PDM_DATA0			8		
	GPT1_3			9		
	DCAN_RX			10		
	SDMMC_WP			11		
	SPI0_CS4			16		
	I2S_BCLK			17		
	GPT1_1_N			18		
	SDIO_D1			19		
	COEX_PRIORITY			20		
	GPT0_3_N			21		
	GPT1_PRE_EVENT			22		
	ANT_SEL_0			23		
	CCA			24		
	COEX_GRANT			26		
	I2C1_CLK			28		
	SDMMC_POW2			29		
GPIO5	ADC3	I/O	VIO1		PU	Hi-Z, Pull, Drive
	xSPI_RESET_RAM			1		
	SDMMC_POW2			3		
	SPI1_POCI			4		
	UART1_TX			5		
	I2C0_CLK			6		
	I2S_MCLK			7		
	PDM_BCLK			8		
	GPT1_2			9		
	DCAN_TX			10		
	SPI0_CS4			16		
	GPT1_0_N			18		
	SDIO_D0			19		
	COEX_REQ			20		
	GPT0_2_N			21		
	I2C1_DATA			28		

GPIO No.	SIGNAL NAME	SIGNAL TYPE [1]	IO RING	PIN MUX ENCODING	PAD STATES	
					RESET	LPDS [2]
GPIO11	ADC0	I/O	VIO1		PU	Hi-Z, Pull, Drive
	UART1_RX			1		
	SDMMC_DATA_2			3		
	SPI1_CS1			4		
	UART1_CTS			5		
	I2C1_CLK			6		
	I2S_DATA0			7		
	PDM_DATA0			8		
	GPT1_1			9		
	DCAN_TX			10		
	SPI0_CS2			16		
	GPT1_2_N			18		
	SDIO_D2			19		
	COEX_REQ			20		
	CCA			24		
GPIO10	ADC1	I/O	VIO1		PU	Hi-Z, Pull, Drive
	UART1_TX			1		
	SDMMC_DATA_3			3		
	SPI1_CLK			4		
	UART1_RTS			5		
	I2C1_DATA			6		
	I2S_DATA1			7		
	PDM_DATA1			8		
	GPT1_0			9		
	DCAN_RX			10		
	SPI0_CS3			16		
	GPT1_3_N			18		
	SDIO_D3			19		
	COEX_PRIORITY			20		
	COEX_GRANT			21		
	CCA			24		
GPIO14	SDMMC_CLK	I/O	VIO1	3	PU	Hi-Z, Pull, Drive
	SPI1_CLK			4		
	UART1_TX			5		
	UART0_RX			6		
	GPT1_0			9		
	SPI0_CS2			16		
	GPT1_PRE_EVENT			17		
	GPT1_1_N			18		
	SDIO_D0			19		
	COEX_GRANT			20		
GPIO13	SDMMC_DATA_0	I/O	VIO1	3	PU	Hi-Z, Pull, Drive
	SPI1_PICO			4		
	UART1_CTS			5		
	UART0_TX			6		
	I2S_BCLK			7		
	I2S_MCLK			8		
	GPT1_3			9		
	GPT1_2_N			18		
	SDIO_CMD			19		
	COEX_PRIORITY			20		
	ANT_SEL_0			23		

GPIO No.	SIGNAL NAME	SIGNAL TYPE[1]	IO RING	PIN MUX ENCODING	PAD STATES	
					RESET	LPDS[2]
GPIO18	SPI0_POCI	I/O	VIO1	4	PU	Hi-Z, Pull, Drive
	UART0_RX			5		
	I2C0_DATA			6		
	I2S_DATA0			7		
	PDM_DATA1			8		
	GPT0_2			9		
	DCAN_TX			10		
	SPI1_CS4			16		
	SDIO_OOB_IRQ			17		
	GPT0_0_N			18		
	COEX_REQ			20		
	GPT1_2_N			21		
GPIO17	SDMMC_WP	I/O	VIO1	1	PU	Hi-Z, Pull, Drive
	SPI0_CLK			4		
	UART0_TX			5		
	I2C0_CLK			6		
	I2S_DATA1			7		
	PDM_DATA0			8		
	GPT0_1			9		
	SPI1_CS3			16		
	SDIO_OOB_IRQ			17		
	GPT0_0_N			18		
	COEX_GRANT			20		
	GPT1_1_N			21		
GPIO16	SPI0_CS1	I/O	VIO1	4	PU	Hi-Z, Pull, Drive
	UART0_RTS			5		
	I2C1_DATA			6		
	I2S_WCLK			7		
	PDM_BCLK			8		
	GPT0_0			9		
	SPI1_CS2			16		
	GPT0_1_N			18		
	SDIO_D2			19		
	GPT1_0_N			21		
	GPT_INFRARED			22		
GPIO19	SPI0_PICO	I/O	VIO1	4	PU	Hi-Z, Pull, Drive
	UART0_CTS			5		
	I2C1_CLK			6		
	I2S_BCLK			7		
	PDM_DATA0			8		
	GPT0_3			9		
	DCAN_RX			10		
	GPT0_PRE_EVENT			16		
	SDIO_OOB_IRQ			17		
	GPT0_1_N			18		
	SDIO_D3			19		
	COEX_PRIORITY			20		
	GPT1_3_N			21		
	GPT_INFRARED			22		

3. Electrical Characteristic

(Test conditions: Ta = 25 ℃, VDD =3.3V internal DC-DC regulator）

3.1. BLE Radio Characteristics，BLE 1Mbps

- Modulation mode：GFSK
- Frequency range：2400～2483.5MHz（2.4G ISM Frequency band）
- IC Transmitting power range： 0～+20dBm typical （Controlled by software programming 0,5,10,20dBm）
- RF receiving sensitivity of antenna feeder: -99.4dBm typical (PER <30.8%)

BLE 1Mbps (LE 1M) Receiver Characteristics			
Receiver sensitivity[2]	PER <30.2%, 37-byte packets	–99.4	dBm
Receiver sensitivity[2]	PER <30.2%, 255 byte-packets	–98.1	dBm

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Receiver saturation	PER <30.2%		0		dBm
Co-channel rejection[1]	Wanted signal at -67 dBm, modulated interferer in channel		10		dB
Selectivity, ±1 MHz[1]	Wanted signal at -67 dBm, modulated interferer at ±1 MHz		0 / 0		dB
Selectivity, ±2 MHz[1]	Wanted signal at -67 dBm, modulated interferer at ±2 MHz.		-35 / -28		dB
Selectivity, ±3 MHz[1]	Wanted signal at -67 dBm, modulated interferer at ±3 MHz		-38 / -32		dB
Selectivity, ±4 MHz[1]	Wanted signal at -67 dBm, modulated interferer at ±4 MHz		-45 / -40		dB
Out-of-band blocking	30 MHz to 2000 MHz, Wanted signal at -67 dBm		–23		dBm
Out-of-band blocking	2003 MHz to 2399 MHz, Wanted signal at -67 dBm		–30		dBm
Out-of-band blocking	2484 MHz to 2997 MHz, Wanted signal at -67 dBm		–30		dBm
Out-of-band blocking	3000 MHz to 6 GHz, Wanted signal at -67 dBm		–21		dBm
Intermodulation	Wanted signal at 2402 MHz, -64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level		–40		dBm
RSSI accuracy	Dynamic range of -90 to -20dBm	-4		4	dB

3.2. Wifi Radio characteristics

Agreement	IEEE 802.11b/g/n/ax
Port	SDIO/SPI/UART/I2C
Frequency range	2.412GHz~2.472GHz、5.180GHz~5.845GHz
TX power	WLAN Performance: 2.4-GHz Transmitter Power @1 Mbps DSSS: 20.5 dBm @6 Mbps OFDM: 20.2 dBm @54 Mbps OFDM: 14 dBm @HT MCS0 MM: 20.2 dBm @HT MCS7 MM: 14 dBm @HE MCS0: 20.2 dBm @HE MCS7: 14 dBm

	WLAN Performance: 5-GHz Transmitter Power @6 Mbps OFDM: 18.5 dBm @54 Mbps OFDM: 10 dBm @HT MCS0 MM: 18dBm @HT MCS7 MM: 10 dBm @HE MCS0: 17.5 dBm @HE MCS7: 10 dBm
Receive sensitivity	WLAN Performance: 2.4-GHz Receiver Characteristics (Sensitivity: 8% PER for 11b rates, 10% PER for 11g/n/ax rates) @1 Mbps DSSS -98 dBm @2 Mbps DSSS -95.3 dBm @11 Mbps CCK -90 dBm @6 Mbps OFDM -93.2 dBm @54 Mbps OFDM -75.5 dBm @HT MCS0 MM 4K -93 dBm @HT MCS7 MM 4K -72.9 dBm @HE MCS0 4K -92.7 dBm @HE MCS7 4K -72.5 dBm WLAN Performance: 5-GHz Receiver Characteristics (Sensitivity: 8% PER for 11b rates, 10% PER for 11g/n/ax rates) @6 Mbps OFDM -92.2 dBm @54 Mbps OFDM -75.1 dBm @HT MCS0 MM 4K -91.4 dBm @HT MCS7 MM 4K -72.7 dBm @HE MCS0 20MHZ -89.5 dBm @HE MCS7 20MHZ -70.4 dBm

3.3. Absolute Maximum Ratings

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to ground, unless otherwise noted

Rated value	MIN	MAX	Unit
VBAT	-0.5	4.2	V
VIO	-0.5	3.6	V
Other terminal voltage	VSS-0.5	VIO+0.5	V
Storage temperature	-40	+150	°C

3.4. ESD Ratings

			Value	Unit
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	RF PIN	±1000	V
		NOT RF PIN	±2000	
	Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002	RF PIN	±250	
		NOT RF PIN	±500	

3.5. Recommended Operating Conditions

Power supply voltage noise should be less than 10mVpp, too large power supply noise, will reduce the RF performance.

Rated value	MIN	Type	MAX	Unit
VBAT	3	3.3	3.6	V
VIO ①	1.62/3	1.8/3.3	1.98/3.6	V
Operating temperature	-40		+85	°C

Note：①VIO PIN can be set to 1.8V or 3.3V。

3.6. GPIO DC Characteristics

Parameter	test condition	MIN MAX	Unit
VIH		0.65 x VIO VIO	V
VIL		0 0.35xVIO	
VOH	4mA	VIO-0.45 VIO	
VOL	4mA	0 0.45	

3.7. 32.768k clock

PARAMETER		Description	MIN	TYP	MAX	UNIT
	Input slow clock frequency	Square wave		32768		Hz
	Frequency accuracy	Inital + temperature + aging			±250	ppm
	Input Duty cycle		30	50	70	%
T_r/T_f	Rise and fall time	10% to 90% (rise) and 90% to 10% (fall) of digital signal level			100	ns
V_{IL}	Input low level		0		0.35 x V_{IO}	V
V_{IH}	Input high level		0.65 x V_{IO}		1.95	V
	Input impedence		1			MΩ
	Input capacitance				5	pF

3.8. Timing Requirements

3.8.1、SDIO default Timing：

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK		26	MHz
t_{WH}	High Period	10		ns
t_{WL}	Low Period	10		
t_{TLH}	Rise time, CLK		10	
t_{THL}	Fall time, CLK		10	
t_{ISU}	Setup time, input valid before CLK ↑	3		
t_{IH}	Hold time, input valid after CLK ↑	2		
t_{ODLY}	Delay time, CLK ↓ to output valid		14.8	
t_{OH}	Output Hold Time	2.5		
C_L	Capacitive load on outputs		15	pF

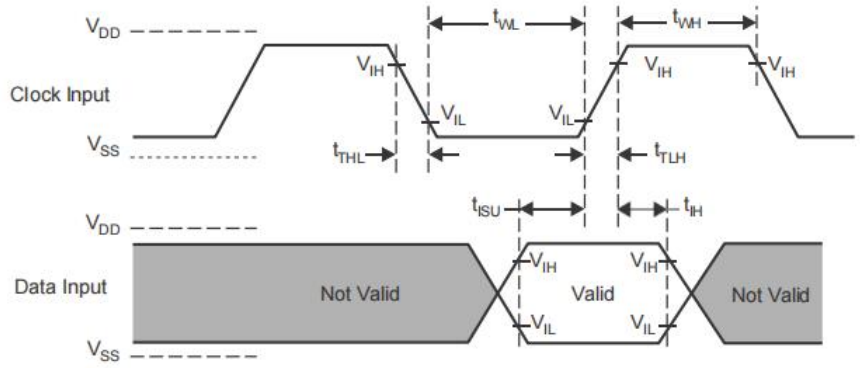


Figure 6-3. SDIO Default Input Timing

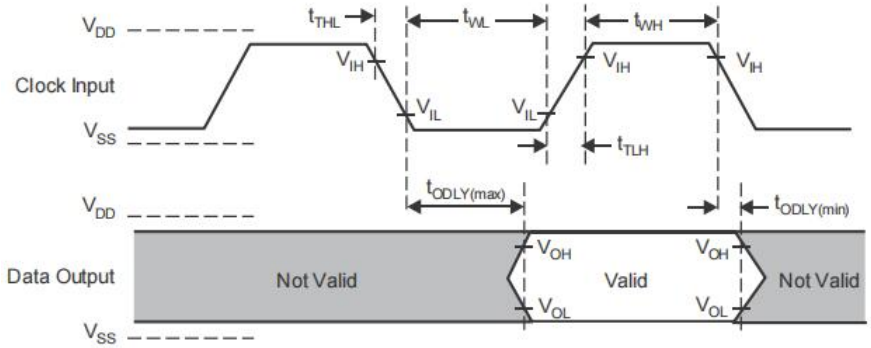


Figure 6-4. SDIO Default Output Timing

3.8.2、SDIO high speed Timing：

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK		52	MHz
t_{WH}	High Period	7		ns
t_{WL}	Low Period	7		
t_{TLH}	Rise time, CLK		3	
t_{THL}	Fall time, CLK		3	
t_{ISU}	Setup time, input valid before CLK ↑	3		
t_{IH}	Hold time, input valid after CLK ↑	2		
t_{ODLY}	Delay time, CLK ↓ to output valid		14	
t_{OH}	Output Hold Time	2.5		
C_L	Capacitive load on outputs		10	pF

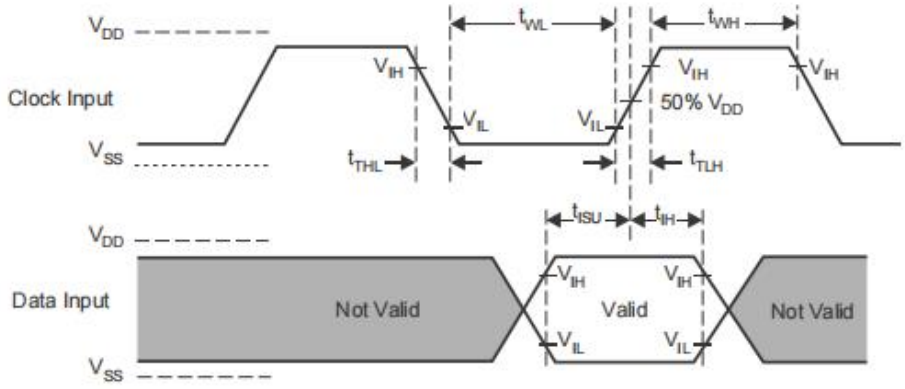


Figure 6-5. SDIO High Speed Input Timing

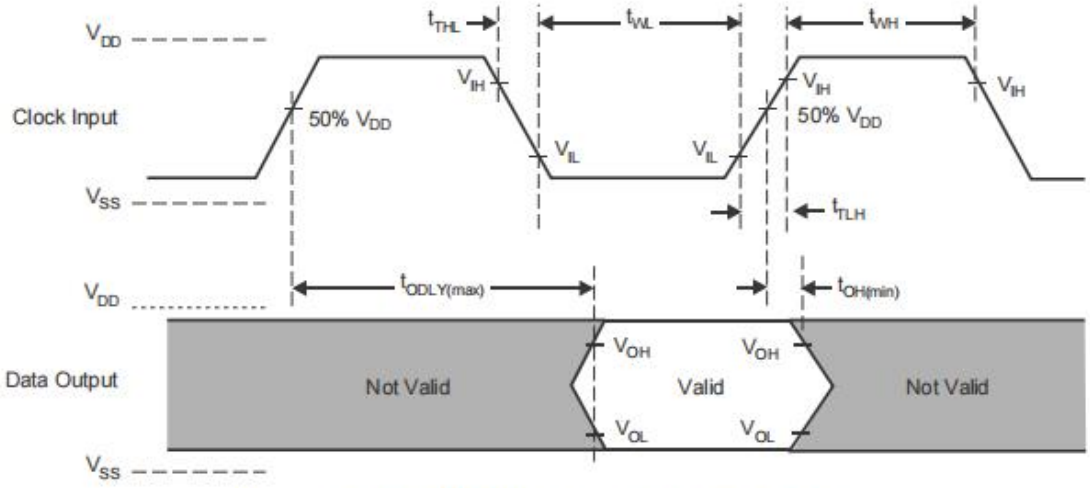
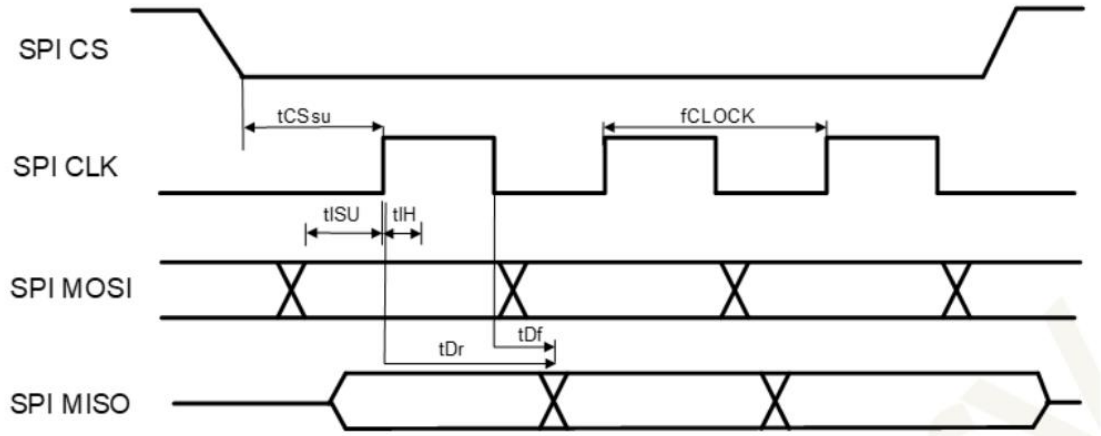


Figure 6-6. SDIO High Speed Output Timing

3.8.3 SPI Timing：

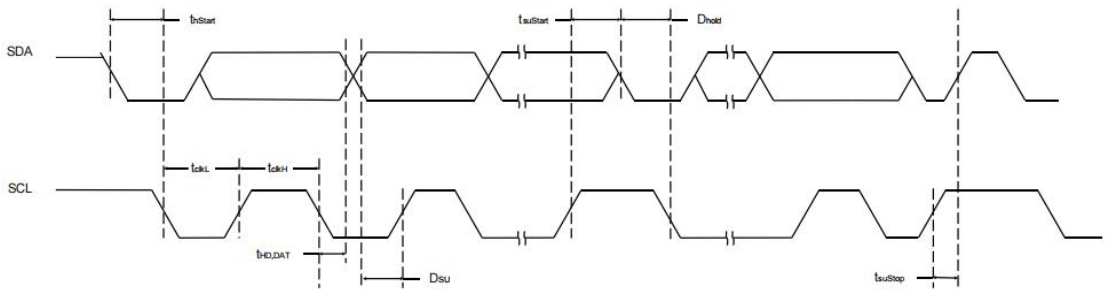


PARAMETER	DESCRIPTION	MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK		80	MHz
t_{High}	High Period	10		ns
t_{Low}	Low Period	10		
t_{TLH}	Rise time, CLK		3	
t_{THL}	Fall time, CLK		3	
t_{CSsu}	CS Setup time, CS valid before CLK ↑	3		
t_{ISU}	PICO, input valid before CLK ↑	3		
t_{IH}	PICO Hold time, input valid after CLK ↑	3		
t_{Dr}, t_{Df} - Active	Delay time, CLK ↑/↓ to output valid	2	10	
t_{Dr}, t_{Df} - Sleep	Delay time, CLK ↑/↓ to output valid		12	
C_L	Capacitive load on outputs	15	40	pF

3.8.3 UART Timing：

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Baud rate		37.5		4364	kbps
Baud rate accuracy per byte	Receive/Transmit	-2.5		+1.5	%
Baud rate accuracy per bit	Receive/Transmit	-12.5		+12.5	%
CTS low to TX_DATA on		0	2		ms
CTS high to TX_DATA off	Hardware flow control			1	Byte
CTS high pulse width		1			bit
RTS low to RX_DATA on		0	2		ms
RTS high to RX_DATA off	Interupt set to 1/4 FIFO			16	Byte

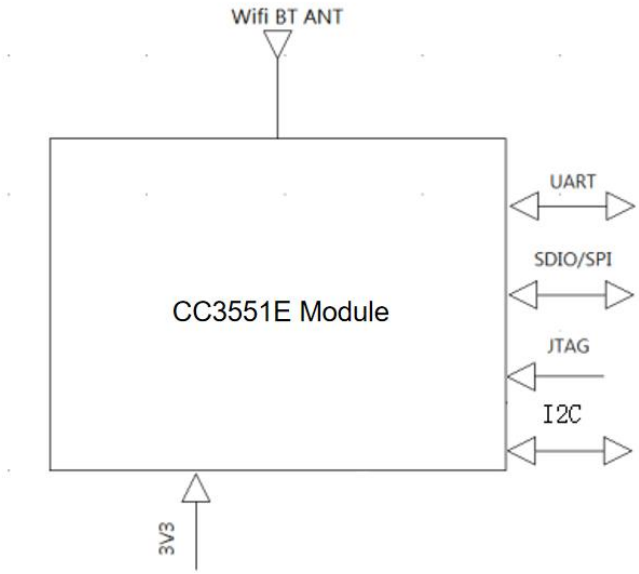
3.8.4 I2C Timing：



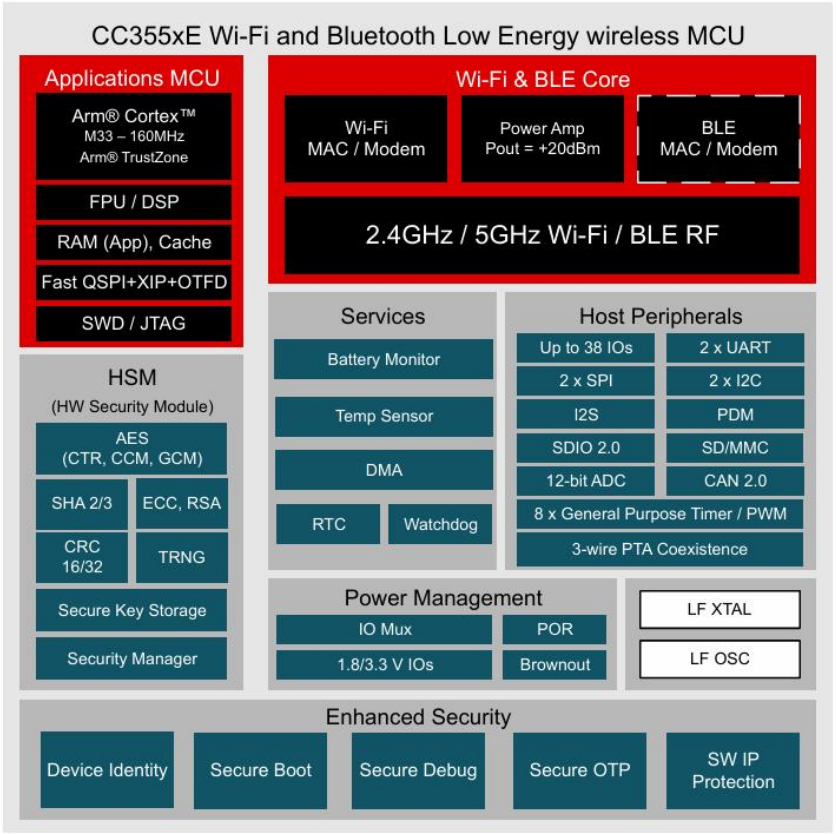
3.9. Working current

TBD

4. Block Diagram



5. IC Functional Block Diagram



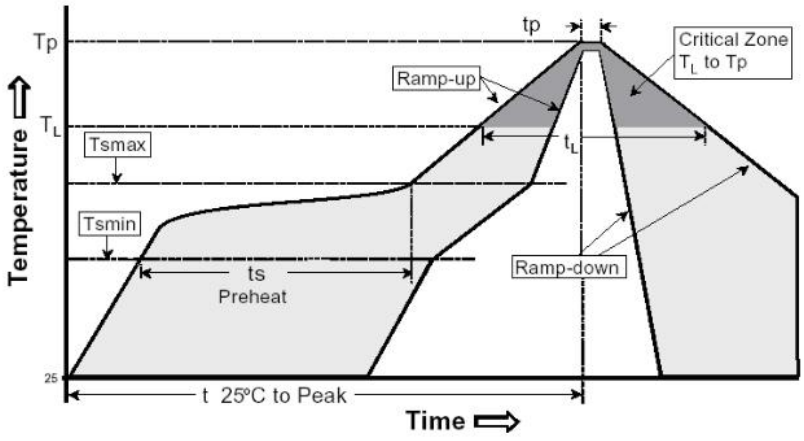
6. Recommended Reflow Curve

Profile Feature	Pb-Free Assembly	
	Large Body	Small Body
Average ramp-up rate(T_L to T_P)	3˚C/second max	
Preheat -Temperature Min (Ts_{min}) -Temperature Max (Ts_{max}) -Time (min to max)(ts)	150˚C 200˚C 60-180 seconds	
$Ts_{max}$to T-$_L$ -Ramp-up Rate	3˚C/second max	
Time maintained above -Temperature (T_L) -Time (t_L)	217˚C 60-150 seconds	
Peak Temperature (T_P)	245 +0/-5˚C	250 +0/-5˚C
Time within 5˚C of actual Peak Temperature (t_p)	10-30 seconds	20-40 seconds
Ramp-down Rate	6˚C/second max	
Time 25˚C to Peak Temperature	8 minutes max	

Notes：

1、lead-free solder paste: Sn 96.5%, Ag 3%, Cu 0.5%)；

2、The furnace temperature curve is for reference only, please adjust according to the actual effect；

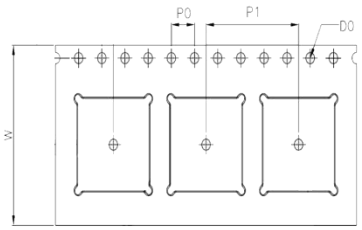


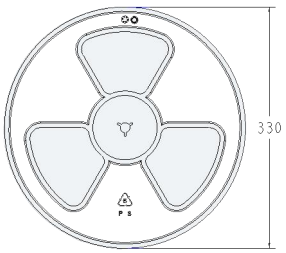
7. Packing Information

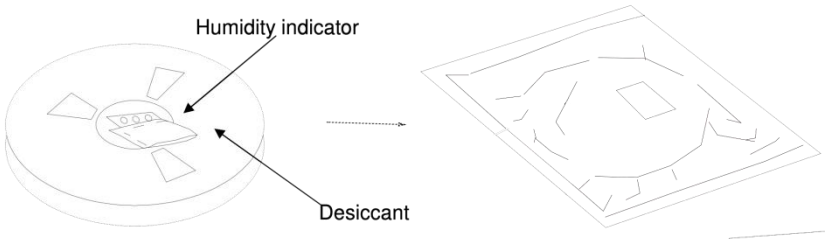
There are two types of module packaging, namely taping and tray. The details are as follows：

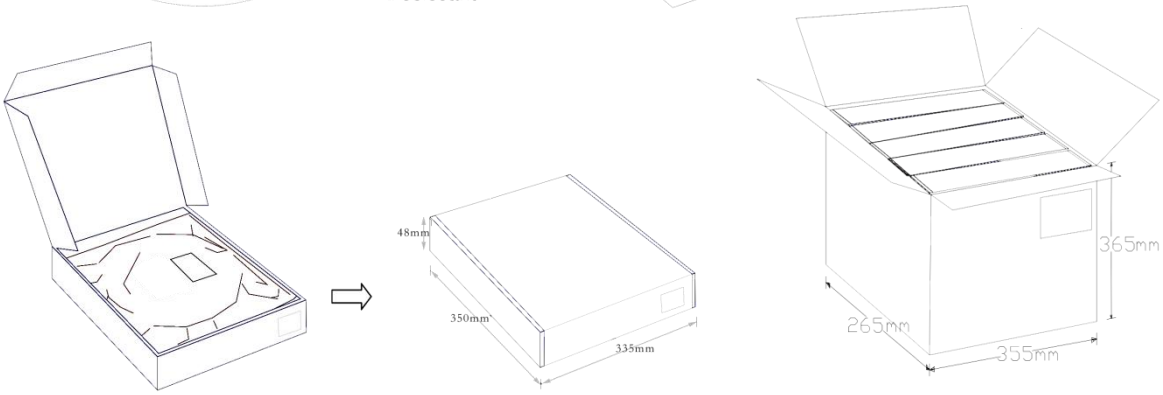
7.1. Tape Packing

The module is delivered to the customer in tape packing(1200pcs/package), packing method and size are as follows:





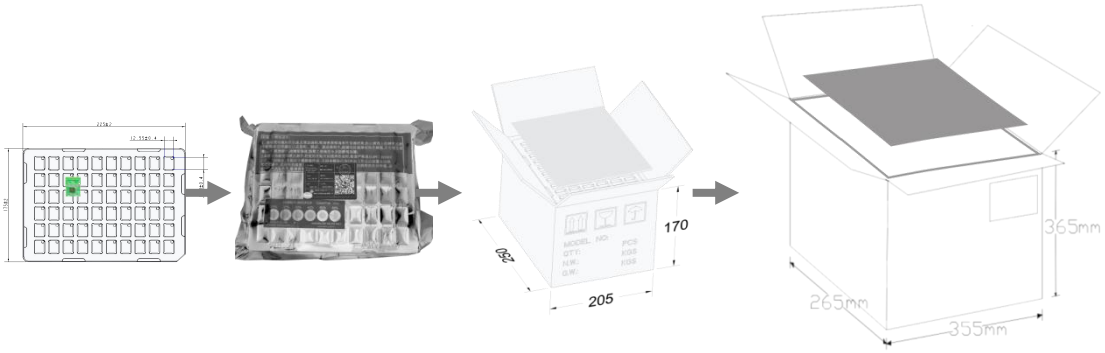




7.2. Reel Packing

The module is delivered to the customer in reel packing(1800pcs/ package), packing method and size are as follows:

60 pcs per plate　15 plates per pack　2 packs per small box　2 small boxes per large

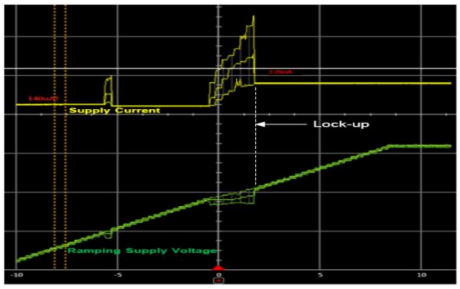


7.3. Humidity Sensitivity Level

Modules are delivered in packing that conforms to moisture sensitivity level 3 (MSL3) requirements.

8. Application Precautions

- Pay attention to electrostatic protection: During the operation, ensure that the instrument and equipment are completely grounded. Prevent poor grounding of the soldering iron and various equipment; avoid static electricity generated by packaging materials and human body contact, which will damage the IC or the program will be blown away; when manually soldering the module, pay attention to the temperature of the soldering iron to avoid peeling off of the PCB copper skin; The power supply damages the module; the operator must install the anti-static ring and implement the static protection inspection to prevent human contact from damaging the IC and the program. Good contact to avoid oxidation and poor contact; the electrostatic voltage of the environment and personnel is within 0±100V. Anti-static signs should be made in the work area.
- Pay attention to avoid program runaway or IC damage caused by abnormal voltage of the Bluetooth chip due to poor power supply circuit of the motherboard, soldering short circuit connection/open circuit.
- When burning the program firmware in the module flash memory, the VDDS DC power supply voltage must be between 2.4~3.3V.
- Avoid multiple occurrences of the power supply voltage falling within the range of the electrical detection threshold (1.76 V ~ 1.78 V) within the BOD Brown-Out Decect range,the below picture shows the power-off lock area, the firmware may be locked causing the boot code to pause and unable to connect to the JTAG protocol. In this state, the reset pin action can be used to eliminate this phenomenon below 1.0 V; the rechargeable battery is in the state of charging and discharging; while applying it, ensure the voltage setting of the protection system, and pay attention to the internal resistance and line impedance voltage drop caused by power supply; ensure The device operates from 2.0 V to 3.6 V with a guaranteed voltage slope greater than 0.5 V/ms (passing the BOD threshold).



- During the production and transportation process, please take good measures to

protect the module parts to prevent the precision parts on the module from being damaged (reflow furnace outlet and assembly, testing, and transportation processes, it is recommended to use anti-collision materials for buffering, and do not collide with each other.

- This module is a humidity-sensitive component. If it is used in SMD reflow soldering operations, please strictly follow the regulations of IPC/JEDECJ-STD-020, and do a good job of drying and dehumidification first, and because this module has been placed after 2 processing operations In the functional test environment, the humidity inside the chip cannot be guaranteed at a certain ratio, please understand;

The above precautions are as follows:

9. Document Revision History

Version	Date	reviser	auditor	Revised content
V1.0	2025/05/06	YDQ	LSC	First release
V1.1	2025/10/15	YDQ	LSC	Update the hardware model to SR-355101PC2N/SR-355102IC2N